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EXAMINER	
MAIS, MARK A	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/690,324	LEE, JI YOUNG	
	Examiner	Art Unit	
	MARK A. MAIS	2619	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-72* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-72* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4, 8-54, and 58-72 are rejected under 35 U.S.C. 102(e) as being anticipated by Ollivier et al. (USP 6,738,881).

3. With regard to claim 1, Ollivier et al. discloses a system for transferring a signal to a channel **[Abstract; DMA controller]**, comprising:

a storage unit **[Fig. 6, each channel i has source register 650, destination register 652, and enable register 654; col. 9, lines 46-53; *See also* control registers, col. 11, line 59 to col. 13, line 7]** associated with the channel **[Fig. 6, channel i; Fig. 4, channels controllers 410, 411, 412; col. 7, lines 12-13; six channels, col. 5, lines 15-18]** for storing source identification information **[Fig. 6, identification is source descriptor 650, destination descriptor 652, and**

enable descriptor 654; col. 9, lines 46-53; Table 3, lines 25-33]of a plurality of sources **[Fig. 4, Resource 0 and 1]** *and indicating an order of priority of the plurality of sources for access to the channel* **[schedulers uses the enable/disable priority algorithm for specific ports, col. 11, lines 35-57 and col. 12, lines 49-54; channel priority fields are overlaid onto the round-robin scheme allowing transfer of high priority channels over low priority channels, col. 12, line 55 to col. 13, line 7]**;

a plurality of selection circuits **[Fig. 4, schedulers 420, 421; col. 7, lines 19-35]** for receiving input signals from the sources, each of the selection circuits selecting one of the plurality of input signals **[Fig. 4, port multiplexers within schedulers 420, 421 col. 7, lines 19-35; *See also* col. 5, lines 38-40]**; and

a circuit for checking outputs of the selection circuits and forwarding selected input signals to the channel **[Fig. 4, port controller 460 and memory interface 472; col. 7, lines 50-52]**, such that the signal is forwarded to the channel according to the priorities associated with the sources **[each channel is given a priority, col. 12, lines 55 to col. 13, line 7; col. 6, lines 44-48]**.

4. With regard to claim 23, Ollivier et al. discloses a system for transferring a signals to channels **[Abstract; DMA controller]**, comprising;

a plurality of storage units **[Fig. 6, each channel i has source register 650, destination register 652, and enable register 654; col. 9, lines 46-53; *See also* control registers, col. 11, line 59 to col. 13, line 7]**, each storage unit being associated with one of the channels **[Fig. 6, channel i; Fig. 4, channels controllers 410, 411, 412; col. 7, lines 12-13; six channels, col. 5,**

lines 15-18], and each storage unit being adapted to store source identification information for each of the sources that can transfer input signals to the associated channel **[Fig. 6, identification is source descriptor 650, destination descriptor 652, and enable descriptor 654; col. 9, lines 46-53; Table 3, lines 25-33]** *and indicating an order of priority of the sources for access to the channel* **[schedulers uses the enable/disable priority algorithm for specific ports, col. 11, lines 35-57 and col. 12, lines 49-54; channel priority fields are overlaid onto the round-robin scheme allowing transfer of high priority channels over low priority channels, col. 12, line 55 to col. 13, line 7]**;

for each of the plurality of channels, a plurality of selection circuits **[Fig. 4, schedulers 420, 421; col. 7, lines 19-35]** for receiving input signals from the sources **[Fig. 4, Resource 0 and 1]**, each of the selection circuits selecting one of the plurality of input signals **[Fig. 4, port multiplexers within schedulers 420, 421 col. 7, lines 19-35; *See also* col. 5, lines 38-40]**; and

for each of the plurality of channels, a circuit for checking outputs of the selection circuits and forwarding selected input signals to the channel **[Fig. 4, port controller 460 and memory interface 472; col. 7, lines 50-52]**, such that the signals are forwarded to the channels according to the priorities associated with the sources **[each channel is given a priority, col. 12, lines 55 to col. 13, line 7; col. 6, lines 44-48]**.

5. With regard to claim 37, Ollivier et al. discloses a direct memory access (DMA) controller for controlling transfer of signals from input sources to output devices, a plurality of channels being connected to the output devices, the DMA controller **[Abstract; DMA controller]** comprising:

a plurality of storage units **[Fig. 6, each channel i has source register 650, destination register 652, and enable register 654; col. 9, lines 46-53; *See also* control registers, col. 11, line 59 to col. 13, line 7]**, each storage unit being associated with one of the channels **[Fig. 6, channel i; Fig. 4, channels controllers 410, 411, 412; col. 7, lines 12-13; six channels, col. 5, lines 15-18]**, and each storage unit being adapted to store source identification information for each of the sources **[Fig. 4, Resource 0 and 1]** that can transfer input signals to the associated channel **[Fig. 6, identification is source descriptor 650, destination descriptor 652, and enable descriptor 654; col. 9, lines 46-53; Table 3, lines 25-33]** *and indicating an order of priority of the sources for access to the channel* **[schedulers uses the enable/disable priority algorithm for specific ports, col. 11, lines 35-57 and col. 12, lines 49-54; channel priority fields are overlaid onto the round-robin scheme allowing transfer of high priority channels over low priority channels, col. 12, line 55 to col. 13, line 7]**;

for each of the plurality of channels, a plurality of selection circuits **[Fig. 4, schedulers 420, 421; col. 7, lines 19-35]** for receiving input signals from the sources **[Fig. 4, Resource 0 and 1]**, each of the selection circuits selecting one of the plurality of input **[Fig. 4, port multiplexers within schedulers 420, 421 col. 7, lines 19-35; *See also* col. 5, lines 38-40]**; and

for each of the plurality of channels, a circuit for checking outputs of the selection circuits and forwarding selected input signals to the channel **[Fig. 4, port controller 460 and memory interface 472; col. 7, lines 50-52]**, such that the signals are forwarded to the channel according to the priorities associated with the sources **[each channel is given a priority, col. 12, lines 55 to col. 13, line 7; col. 6, lines 44-48]**.

6. With regard to claim 51, Ollivier et al. discloses a method for transferring a signal to a channel **[Abstract; DMA controller]**, comprising:

storing **[Fig. 6, each channel i has source register 650, destination register 652, and enable register 654; col. 9, lines 46-53; *See also* control registers, col. 11, line 59 to col. 13, line 7]** source identification information **[Fig. 6, identification is source descriptor 650, destination descriptor 652, and enable descriptor 654; col. 9, lines 46-53; Table 3, lines 25-33]** for a plurality of sources **[Fig. 4, Resource 0 and 1]** *and indicating an order of priority of the plurality of sources for access to the channel* **[schedulers uses the enable/disable priority algorithm for specific ports, col. 11, lines 35-57 and col. 12, lines 49-54; channel priority fields are overlaid onto the round-robin scheme allowing transfer of high priority channels over low priority channels, col. 12, line 55 to col. 13, line 7]** in a storage unit associated with the channel **[Fig. 6, each channel i has source register 650, destination register 652, and enable register 654; col. 9, lines 46-53]**;

providing a plurality of selection circuits **[Fig. 4, schedulers 420, 421; col. 7, lines 19-35]** for receiving input signals from the sources, each of the selection circuits selecting one of the plurality of input signals **[Fig. 4, port multiplexers within schedulers 420, 421 col. 7, lines 19-35; *See also* col. 5, lines 38-40]**;

with a checking circuit, checking outputs of the selection circuits and forwarding a selected input signal to the channel **[Fig. 4, port controller 460 and memory interface 472; col. 7, lines 50-52]**, such that the signal is forwarded to the channel according to the priorities associated with the sources **[each channel is given a priority, col. 12, lines 55 to col. 13, line 7; col. 6, lines 44-48]**.

7. With regard to claims 2 and 52, Ollivier et al. discloses that each selection circuit selects the selected input signal according to a state of a respective control input to the selection circuit **[low priority channels will remain pending as long as high priority channels need to be triggered, col. 13, lines 2-7]**.

8. With regard to claims 3 and 53, Ollivier et al. discloses that the storage unit is a register **[Fig. 6, each channel i has source register 650, destination register 652, and enable register 654; col. 9, lines 46-53]**.

9. With regard to claims 4 and 54, Ollivier et al. discloses that the storage unit stores the source identification information for the sources in order of priority of the sources for access to the channel **[Fig. 6, each channel i has source register 650, destination register 652, and enable register 654; col. 9, lines 46-53]**.

10. With regard to claims 8 and 58, Ollivier et al. discloses that the circuit checks the outputs of the selection circuits in a predetermined sequence **[round robin, col. 9, lines 9-10]**.

11. With regard to claims 9 and 59, Ollivier et al. discloses that the circuit sequentially checks the outputs of the selection circuits **[round robin, col. 9, lines 9-10]**.

12. With regard to claims 10 and 60, Ollivier et al. discloses that the sequence is determined by an order in which the source identification information of the sources is stored in the storage unit **[each channel is given a priority, col. 12, lines 55 to col. 13, line 7; col. 6, lines 44-48]**.

13. With regard to claims 11 and 61, Ollivier et al. discloses that the circuit checks the outputs of the selection circuits in order of priority of the sources for forwarding input signals to the channel **[each channel is given a priority, col. 12, lines 55 to col. 13, line 7; col. 6, lines 44-48]**.

14. With regard to claims 12 and 62, Ollivier et al. discloses that the system includes a plurality of channels, input signals from the sources being able to be forwarded to the plurality of channels **[Abstract]**.

15. With regard to claims 13 and 63, Ollivier et al. discloses a plurality of storage units associated respectively with the plurality of channels **[Fig. 6, each channel i has source register 650, destination register 652, and enable register 654; col. 9, lines 46-53; also, each channel control has its own FIFO, col. 5, lines 40-42]**.

16. With regard to claims 14 and 64, Ollivier et al. discloses that each of the storage units stores source identification information for sources that are able to forward input signals onto the channel associated with the storage unit **[Fig. 6, each channel i has source register 650, destination register 652, and enable register 654; col. 9, lines 46-53]**.

17. With regard to claims 15 and 65, Ollivier et al. discloses that the selection circuits are multiplexers **[Fig. 4, port multiplexers within schedulers 420, 421 col. 7, lines 19-35; *See also* col. 5, lines 38-40]**.

18. With regard to claims 16 and 66, Ollivier et al. discloses that the multiplexers are ordered according to the sequence of the source identification information stored in the storage unit **[round robin, col. 9, lines 9-10]**.

19. With regard to claims 17 and 67, Ollivier et al. discloses that the multiplexers are ordered according to priorities of the sources for forwarding input signals to the channel **[each channel is given a priority, col. 12, lines 55 to col. 13, line 7; col. 6, lines 44-48]**.

20. With regard to claims 18 and 68, Ollivier et al. discloses that he sources are applied to inputs of the selection circuits according to a predetermined order **[each channel is given a priority, col. 12, lines 55 to col. 13, line 7; col. 6, lines 44-48]**.

21. With regard to claims 19 and 69, Ollivier et al. discloses that the predetermined order depends on priority of the sources for access to the channel **[each channel is given a priority, col. 12, lines 55 to col. 13, line 7; col. 6, lines 44-48]**.

22. With regard to claims 20 and 70, Ollivier et al. discloses that the source identification information is generated according to the predetermined order such that the selection circuits select the sources based on priority of the sources for access to the channel **[each channel is given a priority, col. 12, lines 55 to col. 13, line 7; col. 6, lines 44-48]**.

23. With regard to claims 21 and 71, Ollivier et al. discloses that a channel unit associated with the channel for processing information related to the channel **[Fig. 4, channels controllers 410, 411, 412; col. 7, lines 12-13; six channels, col. 5, lines 15-18]**.

24. With regard to claims 22 and 72, Ollivier et al. discloses that the storage unit is part of the channel unit **[Fig. 6, each channel i has source register 650, destination register 652, and enable register 654; col. 9, lines 46-53]**.

25. With regard to claims 24 and 38, Ollivier et al. discloses that each selection circuit selects the selected input signal according to a state of a respective control input to the selection circuit **[low priority channels will remain pending as long as high priority channels need to be triggered, col. 13, lines 2-7]**.

26. With regard to claims 25 and 39, Ollivier et al. discloses that one or more of the sources are allocated to one or more of the channels **[Abstract]**.

27. With regard to claims 26 and 40, Ollivier et al. discloses that the allocation of the sources to the channels is controllable by controlling storage of source identification information in the storage units **[Fig. 6, each channel i has source register 650, destination register 652, and enable register 654; col. 9, lines 46-53]**.

28. With regard to claims 27 and 41, Ollivier et al. discloses that the storage units are registers **[Fig. 6, each channel i has source register 650, destination register 652, and enable register 654; col. 9, lines 46-53]**.

29. With regard to claims 28 and 42, Ollivier et al. discloses that each of the storage units stores its source identification information for the sources in order of priority of the sources for access to the associated channel **[Fig. 6, each channel i has source register 650, destination register 652, and enable register 654; col. 9, lines 46-53]**.

30. With regard to claims 29 and 43, Ollivier et al. discloses that the selection circuits are multiplexers **[Fig. 4, port multiplexers within schedulers 420, 421 col. 7, lines 19-35; *See also* col. 5, lines 38-40]**.

31. With regard to claims 30 and 44, Ollivier et al. discloses that the multiplexers are ordered according to the sequence of the source identification information stored in the storage unit **[round robin, col. 9, lines 9-10]**.

32. With regard to claims 31 and 45, Ollivier et al. discloses that the multiplexers are ordered according to priorities of the sources for forwarding input signals to the channels **[each channel is given a priority, col. 12, lines 55 to col. 13, line 7; col. 6, lines 44-48]**.

33. With regard to claims 32 and 46, Ollivier et al. discloses that the sources are applied to inputs of the selection circuits according to a predetermined order **[round robin, col. 9, lines 9-10]**.

34. With regard to claims 33 and 47, Ollivier et al. discloses that the predetermined order depends on priority of the sources for access to the channels **[each channel is given a priority, col. 12, lines 55 to col. 13, line 7; col. 6, lines 44-48]**.

35. With regard to claims 34 and 48, Ollivier et al. discloses that the source identification information is generated according to the predetermined order such that the selection circuits select the sources based on priority of the sources for access to the channels **[each channel is given a priority, col. 12, lines 55 to col. 13, line 7; col. 6, lines 44-48]**.

36. With regard to claims 35 and 49, Ollivier et al. discloses a plurality of channel units associated respectively with the plurality of channels for processing information related to the channels **[Fig. 4, channels controllers 410, 411, 412; col. 7, lines 12-13; six channels, col. 5, lines 15-18]**.

37. With regard to claims 36 and 50, Ollivier et al. discloses that each of the storage units is part of one of the channel units **[Fig. 6, each channel i has source register 650, destination register 652, and enable register 654; col. 9, lines 46-53]**.

Claim Rejections - 35 USC § 103

38. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

39. Claims 5-7 and 55-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ollivier et al.

40. With regard to claims 5-7 and 55-57, Ollivier et al. does not specifically disclose that the registers **[Fig. 6, source register 650, destination register 652, and enable register 654]** store the source identifications **[identification is source descriptor 650, destination descriptor 652, and enable descriptor 654; col. 9, lines 46-53; Table 3, lines 25-33]** in a scheme using most significant bits (MSBs) and/or least significant bits (LSBs). However, Applicants have not disclosed that using such a MSB/LSB scheme solves any stated problem or is for any particular purpose other than an optimization of a known method of storing and/or searching for (priority)

flags/indicators **[each channel is given a priority, col. 12, lines 55 to col. 13, line 7; col. 6, lines 44-48]**. Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the storing and search scheme Ollivier et al. because such modifications are considered a mere design choice consideration, which fails to patentably distinguish over the prior art of Ollivier et al. In addition, the changing the scheme to use MSB/LSB for storing and searching for (priority) flags/indicators is interpreted as an optimum value for a known process. A discovery of an optimum value for a known process is obvious engineering. See In re Aller, 105 USPQ 233 (CCPA 1955).

Response to Arguments

41. Applicant's arguments filed on June 27, 2008 have been fully considered but they are not persuasive.

42. Applicants state that Ollivier et al. merely services channels on a round-robin basis **[See Applicants' Amendment dated June 27, 2008, page 13, paragraph 1]**. Applicants also state that Ollivier et al fails to disclose a storage unit which stores sources and order of priority of sources for access to the channel **[See Applicants' Amendment dated June 27, 2008, page 13, paragraph 2 to page 14, paragraph 1]**. Applicants argue, apparently, that the output channel in Ollivier et al. does not store priority of sources or that the inputs are forwarded to the output channel according to priorities **[See Applicants' Amendment dated June 27, 2008, page 14, paragraph 2]**. The examiner respectfully disagrees.

43. As noted in the rejection of claim 1 above, each channel has a source register 650, destination register 652, and enable register 654 **[Fig. 6; col. 9, lines 46-53; *See also* control registers, col. 11, line 59 to col. 13, line 7]** and channel controllers 410, 411, and 412 **[Fig. 4,; col. 7, lines 12-13; six channels, col. 5, lines 15-18]**. Each stores identification as source descriptor 650, destination descriptor 652, and enable descriptor 654 **[col. 9, lines 46-53; Table 3, lines 25-33]**. Furthermore, schedulers may use the enable/disable priority algorithm for specific ports **[col. 11, lines 35-57 and col. 12, lines 49-54]** where the channel priority fields are overlaid onto the round-robin scheme allowing transfer of high priority channels over low priority channels **[col. 12, line 55 to col. 13, line 7]**.

Conclusion

44. Accordingly, **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

45. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be

calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

46. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MARK A. MAIS whose telephone number is (571)272-3138. The examiner can normally be reached on M-Th 5am-4pm.

47. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wing F. Chan can be reached on 571-272-7493. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

48. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.
September 22, 2008

/Mark A. Mais/
Examiner, Group Art Unit 2619

/Wing F. Chan/
Supervisory Patent Examiner, Art Unit 2619